SEMESTER-II

COURSE 4: DIGITAL LOGIC DESIGN

Theory **Credits: 3** **3 hrs/week**

Course Objectives

1. Introduce the fundamentals of number systems, their conversions, and binary arithmetic operations.
2. Explore digital logic through gates, Boolean algebra, and simplification techniques for logic functions.
3. Develop proficiency in designing basic combinational circuits like adders and subtractors.
4. Equip students with the skills to implement advanced combinational components such as multiplexers, encoders, and decoders.
5. Foster understanding of sequential circuits, flip-flops, counters, and shift registers for system-level design.

Course Outcomes

At the end of the course, students will be able to:

1. Apply concepts of number systems to perform radix conversions and binary arithmetic using signed and unsigned formats.
2. Simplify logic functions using Boolean algebra, Karnaugh maps, and universal gates.
3. Design and analyze combinational circuits such as half adders, full adders, and subtractors.
4. Construct advanced combinational logic modules, including multiplexers, demultiplexers, encoders, decoders, and their hierarchical versions. Realize complex Boolean functions using combinations of logic modules.
5. Develop and evaluate sequential circuits such as flip-flops, latches, counters, and shift registers.

Unit 1: Number Systems:

Conversion of numbers from one radix to another radix, r's, (r-1)'s complements, signed binary numbers, addition and subtraction of unsigned and signed numbers, weighted and unweighted codes.

Unit 2. Logic Gates and Boolean Algebra:

NOT, AND, OR, universal gates, X-OR and X-NOR gates, Boolean laws and theorems, complement and dual of a logic function, canonical and standard forms, two level realization of logic functions using universal gates, minimizations of logic functions (POS and SOP) using Boolean theorems, K-map (up to four variables), don't care conditions.

Unit 3. Combinational Logic Circuits – 1:
Design of half adder, full adder, half subtractor, full subtractor, ripple adders and subtractors, ripple adder / subtractor.

Unit 4. Combinational Logic Circuits – 2:
Design of decoders, encoders, priority encoder, multiplexers, demultiplexers, higher order decoders, demultiplexers and multiplexers, realization of Boolean functions using decoders, multiplexers.

Unit 5. Sequential Logic Circuits:
Classification of sequential circuits, latch and flip-flop, RS- latch using NAND and NOR Gates, RS, JK, T and D flip-flops, truth tables and excitation tables, conversion of flip- flops, flip-flops with asynchronous inputs (preset and clear). Registers- shift registers, bidirectional shift registers, universal shift register, design of ripple counters, modulus counters.

Text Books:

1. Digital Design, M. Morris Mano, Michael D Ciletti,5th edition, Pearson.
2. Digital Logic Design, K.C. Rao, Ramana, Pen International Press

Reference Books:

1. Digital Electronics and Logic Design, Jaydeep Chakravorty, Universities Press
2. Digital Logic Design, Sonali Singh, BPB Publications

Activities:

Outcome: Apply concepts of number systems to perform radix conversions and binary arithmetic using signed and unsigned formats

Activity: Design a calculator in a spreadsheet or simulation tool (e.g., Logisim) that performs: Decimal ↔ Binary ↔ Hexadecimal conversions and binary arithmetic (addition, subtraction).

Evaluation Method: Rubric-based evaluation on a 10point scale (conversion accuracy, arithmetic correctness)

Outcome: Simplify logic functions using Boolean algebra, Karnaugh maps, and universal gates

Activity: Provide students with complex Boolean expressions and truth tables. Ask them to: Simplify using Boolean laws, Minimize using Karnaugh maps and Implement using only NAND or NOR gates

Evaluation Method: Worksheet submission with step-by-step simplification and evaluation of gate-level implementation using a 10-point scale.

Outcome: Design and analyze combinational circuits such as half adders, full adders, and subtractors

Activity: Build and simulate: Half adder and full adder using logic gates, and half and full subtractor circuits

Evaluation Method: Evaluate the correctness of the circuits for different inputs on a 10-point scale.

Outcome: Construct advanced combinational circuits, including multiplexers, demultiplexers, encoders and decoders.

Activity: Design Multiplexers for function selection, Decoders for control signal generation and Encoders for input compression

Evaluation Method: Project-based evaluation with functional demo and assessments based on a 10-point scale.

Outcome: Develop and evaluate sequential circuits such as flip-flops, latches, counters, and shift registers

Activity: Implement and test SR, JK, D, T flip-flops, asynchronous and synchronous counters using a simulator (E.g. Logisim, Multisim)

Evaluation Method: Lab assessment on a 10-point scale to understand the correctness of the circuit and presentation of the design.

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Practical **Credits: 1** **2 hrs/week**

List of Experiments

The laboratory work can be done by using physical gates and necessary equipment or simulators.

Simulators: https://sourceforge.net/projects/gatesim/ or https://circuitverse.org/ or any free open-source simulator

1. Introduction to digital electronics lab- nomenclature of digital ICs, specifications, study of the data sheet, concept of Vcc and ground, verification of the truth tables of logic gates using TTL ICs.
2. Implementation of the given Boolean functions using logic gates in both SOP and POS forms
3. Realization of basic gates using universal gates.
4. Design and implementation of half and full adder circuits using logic gates.
5. Design and implementation of half and full subtractor circuits using logic gates.
6. Verification of stable tables of RS, JK, T and D flip-flops using NAND gates.
7. Implementation and verification of Decoder and encoder using logic gates.
8. Implementation of 4X1 MUX and DeMUX using logic gates.
9. Implementation of 8X1 MUX using suitable lower order MUX.
10. Implementation of 7-segment decoder circuit.
11. Implementation of 4-bit parallel adder.
12. Design and verification of 4-bit modulus counter.